CLAIMS

What is claimed is:

1. A computer system which includes an apparatus for monitoring the performance of a multithreaded processor, said apparatus comprising:

a processor adapted to execute a plurality of threads simultaneously, each thread including a series of instructions;

a plurality of programmable event counters to count two or more independent events generated by one or more threads of said plurality, said two or more events selected from a predetermined list of events resulting from the normal operation of said processor;

one or more registers to control the operation of said event counters, each register also selecting the events to be counted from said list of events; and

an access location to allow access to said event counters to determine a current count of said events.

2. The computer system of claim 1 wherein said access location allows access to determine said count without disturbing the operation of said counters.

3. The computer system of claim 2 wherein each register comprises a first field of bits for choosing one or more events to be counted.

4. The computer system of claim 3 wherein each register further comprises a second field of bits for choosing one or more events to be masked and not counted.

5. The computer system of claim 4 wherein each register further comprises a third field of bits for choosing from which of said plurality of threads an event is to be counted according to each thread's ID.

6. The computer system of claim 5 wherein said third field of bits can further choose from which of said plurality of threads an event is to be counted according to each thread's current privilege level (CPL).

7. The computer system of claim 6 wherein said counters can be stopped and cleared before a new event is selected.

8. The computer system of claim 7 wherein said counters can be preset to a certain state.

9. The computer system of claim 5 wherein said predetermined list of events includes hardware performance and breakpoint events.

10. An apparatus for monitoring the performance of a multithreaded processor comprising:

processing means for processing a plurality of threads simultaneously, each thread including a series of instructions;

counting means for counting one or more events generated by one or more threads of said plurality, said one or more events selected from a predetermined list of events resulting from the normal operation of said processor;

controlling means for controlling said counting means and for choosing said one or more events from said list; and

accessing means for accessing said counting means to determine the count of said one or more events.

11. The apparatus of claim 10 wherein said counting means comprises a plurality of programmable counters.

12. The apparatus of claim 11 wherein said controlling means comprises one or more registers, each register including a first field of bits for choosing one or more events to be counted.

13. The apparatus of claim 12 wherein each register further comprises a second field of bits for choosing one or more events to be masked and not counted.

14. The apparatus of claim 13 wherein each register further comprises a third field of bits for choosing from which of said plurality of threads an event is to be counted according to each thread's ID.

15. The apparatus of claim 14 wherein said third field of bits can further choose from which of said plurality of threads an event is to be counted according to each thread's current privilege level (CPL).

16. The apparatus of claim 15 wherein said accessing means comprise instruction means within said processor for reading a count from each of said counters.

17. The apparatus of claim 14 wherein said predetermined list of events includes hardware performance and breakpoint events.

18. A method for monitoring the performance of a multithreaded processor, said method comprising:

executing a plurality of threads simultaneously, each thread including a series of instructions;

counting a plurality of independent events generated by one or more threads of said plurality, said plurality of events selected from a predetermined list of events resulting from the normal operation of said processor;

controlling the operation of said event counters, each register also selecting the events to be counted from said list of events; and

accessing said event counters to determine a current count of said events.

19. The method in claim 18 further comprising:

prior to said counting, selecting and qualifying said plurality of independent events to be counted.

20. The method in claim 19 wherein said qualifying includes requiring that said plurality of events have a preselected thread ID.

21. The method in claim 20 wherein said qualifying further includes requiring that said plurality of events have a preselected thread current privilege level (CPL).

22. An apparatus incorporated in an integrated circuit (IC) for monitoring the performance of a multithreaded central processing unit (CPU) by recording the occurrence of events resulting from the normal operation of said CPU, each event comprising an electric signal representing the incidence of a particular activity within said IC, said apparatus comprising:

a processor adapted to execute a plurality of threads simultaneously, each thread including a series of instructions

first and second programmable counters operated synchronously to record first and second selected events respectively;

logic circuitry to couple said first and second selected events to said first and second programmable counters, respectively;

a control register coupled to said logic circuitry to select said first and second selected events; and

an access location to allow access to said counters.

23. The apparatus of claim 22 wherein said logic circuitry comprises one more multiplexers coupled to receive a plurality of events.

24. The apparatus of claim 23 wherein said logic circuitry is adapted to select said first and second selected events from said plurality of events according to their thread ID.